



PATENT 8053-1016

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Kazuhiro NAKAJIMA et al.

Conf. 9942

Application No. 10/625,695

Group 2811

Filed July 24, 2003

Examiner Ori Nadav

PRODUCTION PROCESS FOR PRODUCING SEMICONDUCTOR DEVICES, SEMICONDUCTOR DEVICES PRODUCED THEREBY, AND TEST SYSTEM FOR CARRYING OUT YIELD-RATE TEST IN PRODUCTION OF SUCH SEMICONDUCTOR DEVICES

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying document, a copy of which is attached to this statement, is made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of this item is that this reference was cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2002-279397, filed September 25, 2002. A copy of the Japanese Official Action in which it was cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. An English translation of the enclosed portion is also attached hereto.

Docket No. 8053-1016 Appln. No. 10/625,695

Under the provisions of 37 CFR 1.97(e), undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

Respectfully submitted,

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January 14, 2005

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(Use several sheets if necessary)		Filing Date: July 24, 2003		Group Art Unit: 2811				
		U.S. PATEN	T DOCUMENTS					
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^{*} Abstract provided for the Examiner's convenience

NAKAJIMA et al.

U.S. Application No. 10/625,695

Our. Ref. 8053-1016

Record (See the Reference Citation List to obtain the citation)

Claim 1

Citation 1

Remarks:

In Citation 1, reference is made to an integrated semiconductor circuit, constructed to accomplish probing in the wiring layer process completion stage. Also, accomplishing electrical disconnection in the pad region of each layer is nothing more than that which could be appropriately done by one of ordinary skill in the Art.

Reference Citation List

1. Japanese Laid-Open Patent Application Publication H10-242231 (particular reference is made to Fig.4)

Record of the Examination Results relating to Documents of the Prior Art

· Examined Technical Field: IPC 7th Edition

H01L 21/66

The record of these examination results relating to documents of the prior art do not constitute the grounds for rejection.